Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 17, with the following rewritten paragraph.

--Preferred embodiment of this invention will be explained with reference to the drawings of FIG. 2A to 2E. Referring to FIG. 2A, a semiconductor substrate 201 is provided firstly; for instance silicon dioxide. An oxide layer (not illustrated) is deposited on the semiconductor substrate 201; for instance silicon dioxide. A dielectric layer (not illustrated) is deposited on the oxide layer; for instance silicon nitride. The oxide and nitride layers are defined as a mask layer of an active region in the semiconductor substrate 201. Thereafter, etching a portion of the mask layers through a dry etching process, and dry etching is performed and stopped within the semiconductor substrate 201 so as to form a plurality of shallow trench. Then, the surfaces of shallow trench have an oxidation so that the damage on the shallow trench surface will be filled and repaired. Subsequently, performing trench filling with silicon dioxide by chemical vapor deposition ~~(CMP)~~ (CVD) technique and planarizing the trench oxide layer by chemical mechanical polishing ~~(CMP)~~ (CVD) technique so that a plurality of isolation 203 is formed, which can provide a isolation between each semiconductor device through subsequent processes. Following, a gate structure, which comprises a thin gate oxide 205 and a polysilicon gate electrode 207 thereof, is formed sequentially on the semiconductor substrate 201 and between a pair of isolation 203, wherein the polysilicon gate electrode 207 is formed upon the gate oxide 205.--